REMARKS

Claims 1 through 15 are currently pending in the application.

Claims 2, 3, and 10 are allowed.

This amendment is in response to the Office Action of October 26, 2004.

35 U.S.C. § 112 Claim Rejections

Claims 1 and 15 are rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant has amended the claimed invention to particularly point out and distinctly claim the subject matter of the invention to comply with the provisions of 35 U.S.C. § 112. Therefore, presently amended claims 1 and 15 are allowable under the provisions of 35 U.S.C. § 112.

35 U.S.C. § 102(e) Anticipation Rejections

Anticipation Rejection Based on Yew et al. (U.S. Patent 6,049,129)

Claims 1, 4, 5, 7, 9, and 11 through 14 were rejected under 35 U.S.C. § 102(e) as being anticipated by Yew et al. (U.S. Patent 6,049,129).

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicant has amended the claimed invention to clearly distinguish over the cited prior art.

Applicant asserts that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicant asserts that the Yew et al. reference does not and cannot anticipate the claimed invention of independent claim 1 under 35 U.S.C. § 102 because the Yew et al. reference does not identically describe, either expressly or inherently, each and every element of the claimed invention in as complete detail as contained in the claims.

Turning to the cited prior art, Yew et al. describes a substantially flat high frequency integrated circuit package having substantially the same outline as the silicon chip. (Col. 1, lines 7-9, Col. 3, lines 16-17). The integrated circuit package 30 comprises a silicon chip 50. Printed circuit board 70 is attached to silicon chip 50 by an adhesive layer 60. Printed circuit board 70 consists of three layers, a top layer 72, an intermediate layer 74, and a bottom layer 76. (Col. 3, lines 48-57). Intermediate layer 74 has routing strips 82 that are electrically connected through vias 84 to pads 100 located on top surface 92 of top layer 72. (Col. 4, line 66 - Col. 5, line 2). Intermediate layer 74 includes a pair of bus bars 110. These bus bars are electrically connected through vias 84 to one or more pads 110. (Col. 5, lines 7-9). Silicon chip 50 is connected to routing strips 82 and bus bars 110 through bonding pads 120. (Col. 5, lines 14-17). Connections to the routing strips 82 and bus bars 110 are made through opening 86. (FIG. 2). Bus bars 110 are connected to pads 100 by wire bonding through opening 86. (FIGs. 4 and 5, Col. 8, lines 55-58, lines 60-62).

Applicant asserts that the Yew et al. reference fails to identically describe the elements of the claimed invention calling for "two pieces of adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, a width of one piece of the two pieces of adhesive tape extending at least proximate an edge of said at least one semiconductor die to an edge of said at least one semiconductor substrate opening, a width of another piece of the two pieces of adhesive tape extending at least proximate another edge of said at least one semiconductor substrate opening, a contact area between said at least one semiconductor die and said semiconductor substrate being substantially maximized" as recited in independent claim 1. Applicant asserts that the Yew et al. reference contains no description whatsoever regarding such claim limitations. Applicant further asserts that the Yew et al. reference is silent regarding any such claim limitations. Therefore, the cited prior art does not and cannot anticipate the claimed invention under 35 U.S.C. § 102 regarding the invention of independent claim 1.

Therefore, Applicant asserts that presently amended independent claim 1 is allowable over the cited prior art. In addition, Applicant asserts that claims 4 through 9 and 11 through 14 are allowable at least because each depends either directly or indirectly from claim 1, which is allowable.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on Yew et al. (U.S. Patent 6,049,129) in view of Khandros et al. (U.S. Patent 5,148,266)

Claim 6 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Yew et al. (U.S. Patent 6,049,129) in view of Khandros et al. (U.S. Patent 5,148,266). Applicant respectfully traverses this rejection, as hereinafter set forth.

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicant has amended the claimed invention to clearly distinguish over the cited prior art.

Applicant asserts that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

Applicant asserts that, in the first instance, dependent claim 6 is allowable as depending from an allowable independent claim 1.

Again, turning to the cited prior art, the disclosure of Yew et al. teaches or suggests a substantially flat high frequency integrated circuit package having substantially the same outline as the silicon chip. (Col. 1, lines 7-9, Col. 3, lines 16-17). The integrated circuit package 30 comprises a silicon chip 50. Printed circuit board 70 is attached to silicon chip 50 by an adhesive layer 60. Printed circuit board 70 consists of three layers, a top layer 72, an intermediate layer 74, and a bottom layer 76. (Col. 3, lines 48-57). Intermediate layer 74 has routing strips 82 that are

electrically connected through vias 84 to pads 100 located on top surface 92 of top layer 72. (Col. 4, line 66 - Col. 5, line 2). Intermediate layer 74 includes a pair of bus bars 110. These bus bars are electrically connected through vias 84 to one or more pads 110. (Col. 5, lines 7-9). Silicon chip 50 is connected to routing strips 82 and bus bars 110 through bonding pads 120. (Col. 5, lines 14-17). Connections to the routing strips 82 and bus bars 110 are made through opening 86. (FIG. 2). Bus bars 110 are connected to pads 100 by wire bonding through opening 86. (FIGs. 4 and 5, Col. 8, lines 55-58, lines 60-62).

The Khandros reference teaches or suggests a semiconductor chip assembly having an interposer and flexible leads (Title). The semiconductor chip is mounted to contact pads in a compact area array. An interposer is disposed between the chip and the substrate. The contacts on the chip are connected to terminals on the interposer by flexible leads that extend through openings in the interposer. (Abstract).

Again, Applicant asserts that any combination of the Yew et al. reference and the Khandros et al. reference fails to teach or suggest the claim limitations of for "two pieces of adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, a width of one piece of the two pieces of adhesive tape extending at least proximate an edge of said at least one semiconductor die to an edge of said at least one semiconductor substrate opening, a width of another piece of the two pieces of adhesive tape extending at least proximate another edge of said at least one semiconductor substrate opening, a contact area between said at least one semiconductor die and said semiconductor substrate being substantially maximized" as recited in independent claim 1 as currently amended, from which claim 6 depends through intervening claim 4. Any combination of the Yew et al. and the Khandros et al. reference contains any teaching or suggestion whatsoever regarding such claim limitations. Both the Yew et al. reference and the Khandros et al. reference are silent regarding any such claim limitations. Therefore, any combination of the cited prior art does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the inventions of independent claim 1 as currently amended and dependent claim 6, which depends from claim 1.

Further, Applicant asserts that any rejection of the inventions of currently amended independent claim 1 and dependent claim 6 would be a hindsight reconstruction of the presently claimed inventions based solely upon Applicant's disclosure and not the cited prior art, as any combination of the cited prior art fails to teach or suggest all the claim limitations of the presently claimed inventions. Such a rejection is neither contemplated by nor within the ambit of 35 U.S.C. § 103 and is clearly improper. Further, any such rejection cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the inventions of currently amended independent claim 1 and dependent claim 6, which depends from claim 1.

Therefore, Applicant asserts that currently amended independent claim 1 and dependent claim 6 are allowable over any combination of the cited prior art.

Obviousness Rejection Based on Yew et al. (U.S. Patent 6,049,129) in view of Murakami et al. (U.S. Patent 5,612,569)

Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Yew et al. (U.S. Patent 6,049,129) in view of Murakami et al. (U.S. Patent 5,612,569). Applicant respectfully traverses this rejection, as hereinafter set forth.

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicant has amended the claimed invention to clearly distinguish over the cited prior art.

Applicant asserts that dependent claim 8 is allowable as depending from an allowable independent claim 1.

Again, Applicant asserts that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

Again, turning to the cited prior art, Yew et al. teaches or suggests a substantially flat high frequency integrated circuit package having substantially the same outline as the silicon chip. (Col. 1, lines 7-9, Col. 3, lines 16-17). The integrated circuit package 30 comprises a silicon chip 50. Printed circuit board 70 is attached to silicon chip 50 by an adhesive layer 60. Printed circuit board 70 consists of three layers, a top layer 72, an intermediate layer 74, and a bottom layer 76. (Col. 3, lines 48-57). Intermediate layer 74 has routing strips 82 that are electrically connected through vias 84 to pads 100 located on top surface 92 of top layer 72. (Col. 4, line 66 - Col. 5, line 2). Intermediate layer 74 includes a pair of bus bars 110. These bus bars are electrically connected through vias 84 to one or more pads 110. (Col. 5, lines 7-9). Silicon chip 50 is connected to routing strips 82 and bus bars 110 through bonding pads 120. (Col. 5, lines 14-17). Connections to the routing strips 82 and bus bars 110 are made through opening 86. (FIG. 2). Bus bars 110 are connected to pads 100 by wire bonding through opening 86. (FIGs. 4 and 5, Col. 8, lines 55-58, lines 60-62).

Murakami teaches or suggests a semiconductor device having bonding wires 5 covered with a flexible/fluid substance 20. Mold resin 2A covers flexible/fluid substance 20. The mold resin 2A is bored with a hole 22 at the side opposite to the principal surface of the semiconductor chip 1 to expose a portion of the semiconductor chip 1 to the outside. (FIG. 34, Col. 31, lines 13-17).

Again, Applicant asserts that any combination of the Yew et al. reference, the Murakami reference, and APA (17) fails to teach or suggest the claim limitations of for "two pieces of adhesive tape interposed between and attaching said semiconductor die active surface and said semiconductor substrate first surface, a width of one piece of the two pieces of adhesive tape extending at least proximate an edge of said at least one semiconductor die to an edge of said at least one semiconductor substrate opening, a width of another piece of the two pieces of adhesive tape extending at least proximate another edge of said at least one semiconductor substrate opening, a contact area between said at least one semiconductor die and said semiconductor substrate being substantially maximized" as recited in independent claim 1 as currently amended, from which claim 8 depends through intervening claims 4 and 7. Any combination of the Yew et al. reference and the Murakami reference contains no teaching or suggestion whatsoever regarding such claim limitations. Both the Yew et al. reference and the Murakami reference are

silent regarding any such claim limitations. Therefore, any combination of the cited prior art does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed inventions of presently amended independent claim 1 as well as claim 8, which depends from claim 1.

Further, Applicant asserts that any rejection of the inventions of currently amended independent claim 1 and dependent claim 8 would be a hindsight reconstruction of the presently claimed inventions based solely upon Applicant's disclosure and not the cited prior art, as any combination of the cited prior art fails to teach or suggest all the claim limitations of the presently claimed inventions. Such a rejection is neither contemplated by nor within the ambit of 35 U.S.C. § 103 and is clearly improper. Further, any such rejection cannot and does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the inventions of currently amended independent claim 1 and dependent claim 8, which depends from claim 1.

Therefore, Applicant asserts that independent claim 1 as currently amended and dependent claim 8 are allowable over any combination of the cited prior art.

Applicant submits that claims 1 through 15 are clearly allowable over the cited prior art.

Applicant requests the allowance of claims 1 through 15 and the case passed for issue.

Respectfully submitted,

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